Changes to the Claims

Claims 1-34 (Cancelled).

35. (Currently Amended) A method comprising forming a plurality of row conductors to intersect with a plurality of column conductors at a plurality of intersections, each said intersection including an electrically linear resistive element in series with an unpatterned voltage breakdown element.

36. (Original) The method as defined in Claim 35, wherein the forming a plurality of row conductors to intersect with a plurality of column conductors comprises:

depositing a first layer of column material;

patterning the first layer of column material to form the plurality of column conductors;

forming a voltage breakdown material on the plurality of column conductors;

forming an electrically linear resistive material upon the voltage breakdown material;

patterning the electrically linear resistive material;

depositing a layer of row material upon the patterned electrically linear resistive material;

patterning the layer of row material to form the plurality of row conductors.

37. (Original) The method as defined in Claim 36, further comprising forming an electrical insulator upon the voltage breakdown material and the patterned electrically linear resistive material.

38. (Original) The method as defined in Claim 36, wherein each said intersection has an unpatterned layer of material selected from the group consisting of the electrical insulator and the voltage breakdown material.

39. (Original) The method as defined in Claim 36, wherein:

the electrically linear resistive material is selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the voltage breakdown material comprises an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

40. (Original) The method as defined in Claim 35, wherein the forming a plurality of row conductors to intersect with a plurality of column conductors comprises:

forming a first electrical insulator;

depositing a first layer of column material over the first electrical insulator;

patterning the first layer of column material to form the plurality of column conductors;

forming a first voltage breakdown material on the plurality of column conductors;

forming a first electrically linear resistive material upon the first voltage breakdown material;

depositing a first layer of row material upon the first electrically linear resistive material; and

patterning the first layer of row material to form a first plurality of row conductors;

forming a second electrical insulator upon the first plurality of row conductors;

depositing a second layer of column material over the second electrical insulator;

patterning the second layer of column material to form a second plurality of column conductors;

forming a second voltage breakdown material on the second plurality of column conductors;

forming a second electrically linear resistive material upon the second voltage breakdown material;

depositing a second layer of row material upon the second electrically linear resistive material; and

patterning the second layer of row material to form a second plurality of row conductors.

41. (Original) The method as defined in Claim 40, wherein:

at least one of the first and second electrical insulators is unpatterned;

at least one of the first and second voltage breakdown materials is unpatterned; and

at least one of the first and second electrically linear resistive materials is patterned.

42. (Original) The method as defined in Claim 40, wherein each said intersection has an unpatterned layer of material selected from the group consisting of the first and second electrical insulator and the first and second voltage breakdown materials.

43. (Original) The method as defined in Claim 40, wherein:

the first and second electrically linear resistive materials are selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the first and second voltage breakdown materials comprise an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

44. (Original) The method as defined in Claim 35, wherein the forming a plurality of row conductors to intersect with a plurality of column conductors comprises:

depositing a first layer of row material;

patterning the first layer of row material to form the plurality of row conductors;

forming a first voltage breakdown material on the plurality of row conductors;

forming a first electrically linear resistive material upon the first voltage breakdown material;

depositing a layer of column material upon the first electrically linear resistive material;

patterning the layer of column material to form the plurality of column conductors;

forming a second voltage breakdown material on the plurality of column conductors;

forming a second electrically linear resistive material upon the second voltage breakdown material;

depositing a second layer of row material upon the second electrically linear resistive material; and

patterning the second layer of row material to form another plurality of said row conductors.

45. (Original) The method as defined in Claim 44, wherein:

the first voltage breakdown material, upon which the first electrically linear resistive material is formed, is unpatterned;

the first electrically linear resistive material, upon which the first layer of column material is deposited, is patterned;

the second voltage breakdown material, upon which the second electrically linear resistive material is formed, is unpatterned;

the second electrically linear resistive material, upon which the second layer of row material is deposited, is patterned.

46. (Original) The method as defined in Claim 44, wherein each said intersection has an unpatterned layer of material selected from the group consisting of the first voltage breakdown material and the second voltage breakdown material.

47. (Original) The method as defined in Claim 44, wherein:

the first and second electrically linear resistive materials are selected from the group consisting of lightly doped microcrystalline silicon, lightly doped amorphous silicon, intrinsic silicon, refractory metal silicide nitride; and

the first and second voltage breakdown materials comprise an antifuse having a dielectric with a thickness not greater than 200 Angstroms.

48. (Original) A memory structure made by the method of Claim 35.

49. (Original) The memory structure as defined in Claim 48, further comprising a primary of memory elements, wherein each one said row conductor connected to one said column conductor by one said electrically linear resistive element in series with one said voltage breakdown element.

50. (Original) The memory structure as defined in Claim 49, wherein each said memory element is in a memory device selected from the group consisting of a WORM memory device and a one time programmable memory device.

51. (Original) The memory structure as defined in Claim 49, wherein the memory device is included in a memory apparatus that is selected from the group consisting of a digital film and a memory card.